



**Model Name:GA-78LMT-S2P**

### Component value change history

**Version: 5.02**

**P-Code: U99098-0**

[illegible]

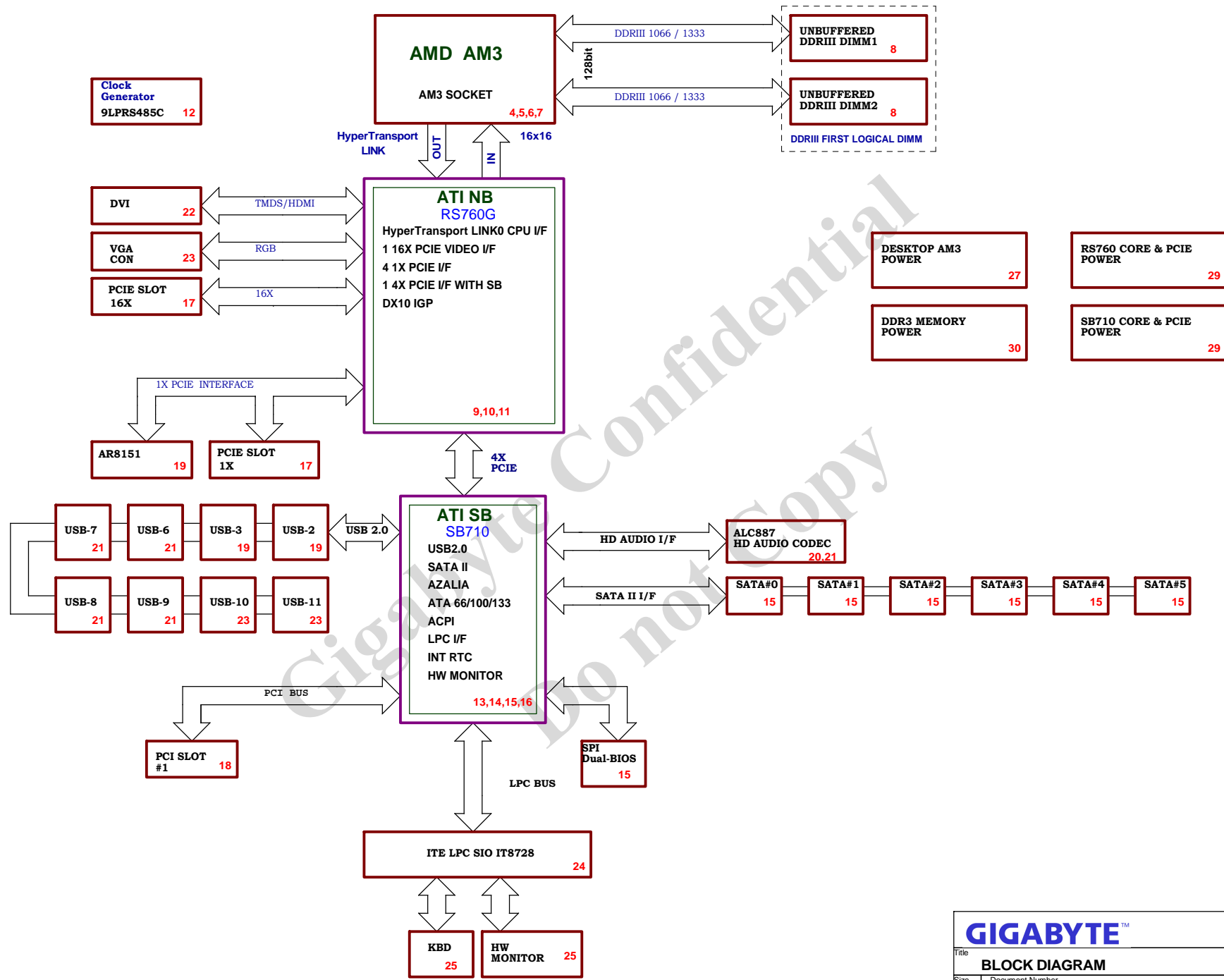
### Circuit or PCB layout change for next version

[illegible]

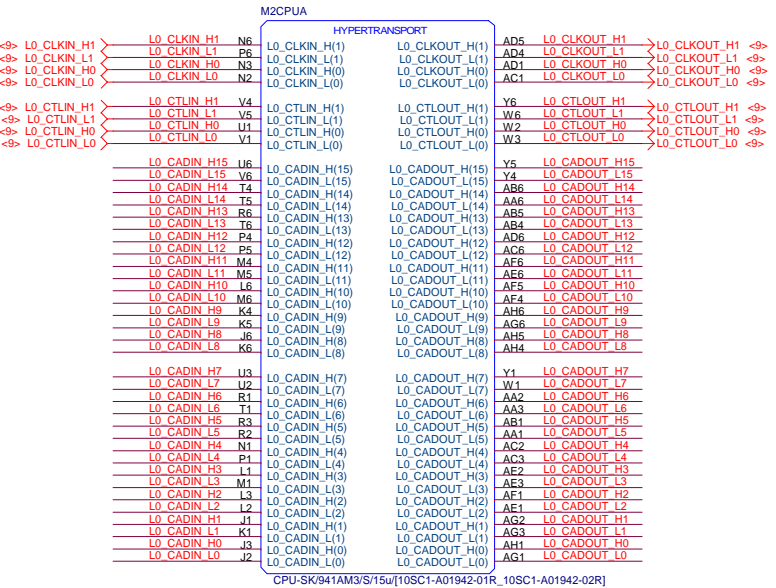
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Title			
<b>BOM &amp; PCB HISTORY</b>			
Size	Document Number	Rev	
Custom	<b>GA-78LMT-S2P</b>	<b>5.02</b>	
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www.xinxunwei.com 400-800-9990  
RS780L CUSTOMER DESKTOP DESIGN

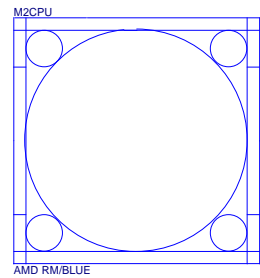


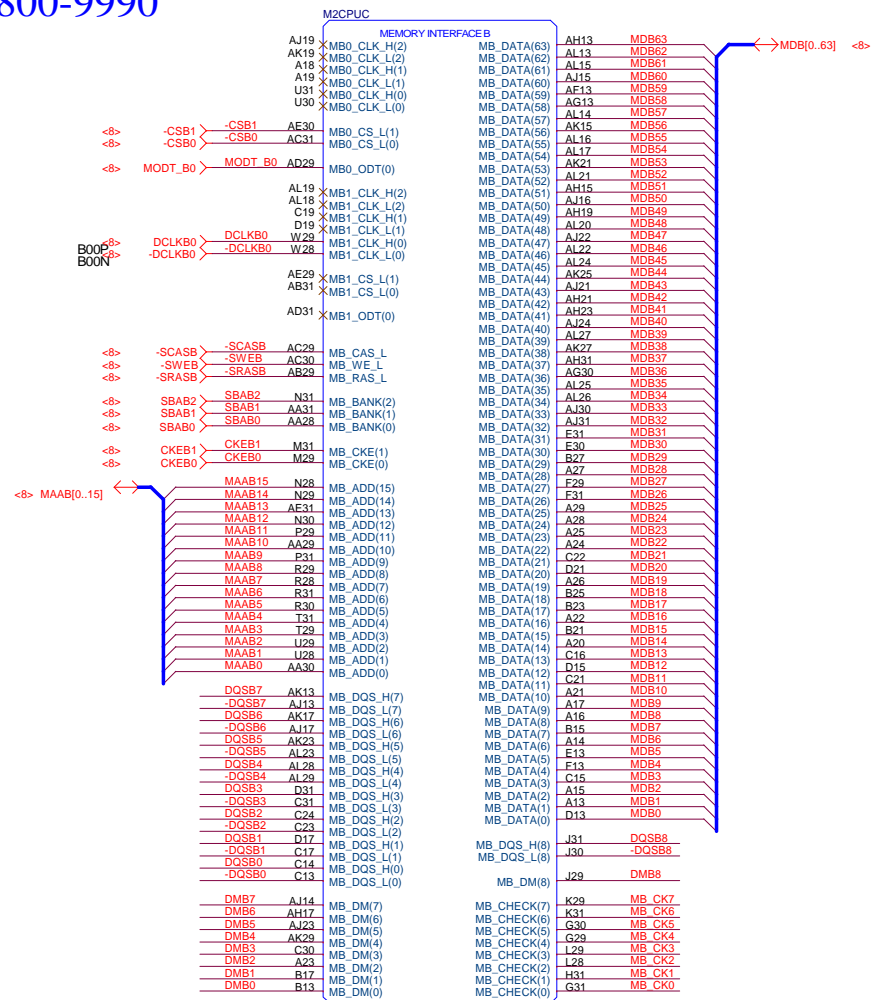
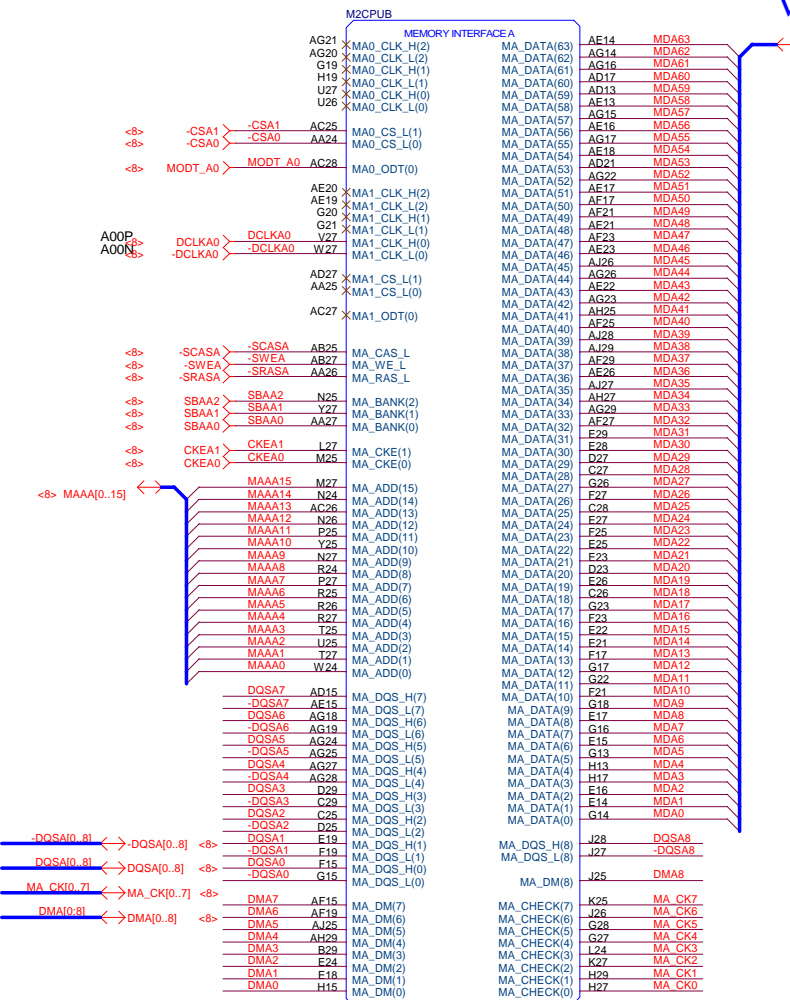
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CPU\_VDD\_RUN = VCORE  
CPU\_VDDA\_RUN = VDDA25  
VLDT\_RUN = VCC12\_HT  
CPU\_VDDIO\_SUS = DDR18V  
CPU\_VTT\_SUS = DDRVTT

VLDT\_A = VCC12\_HT  
VLDT\_B = HT12B

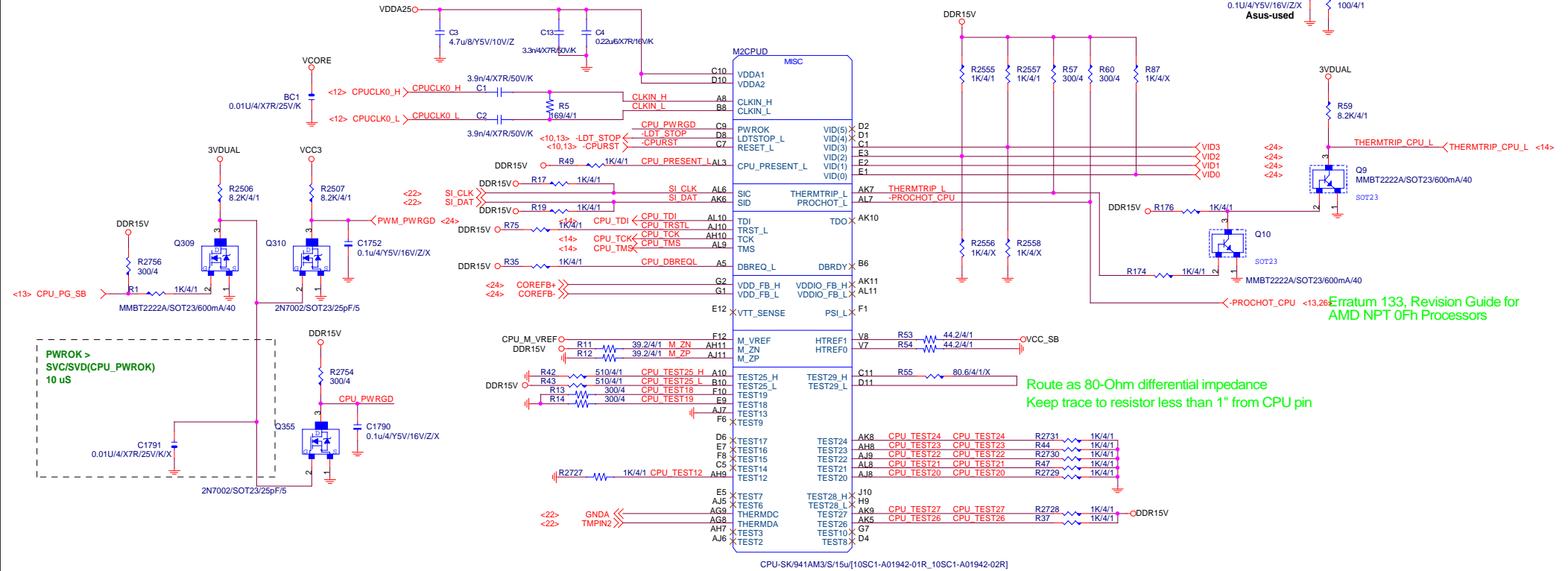
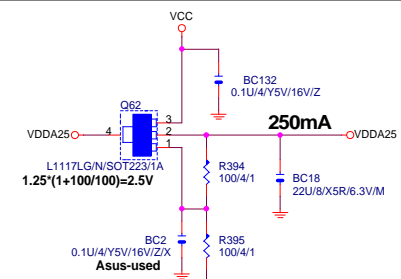
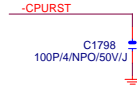
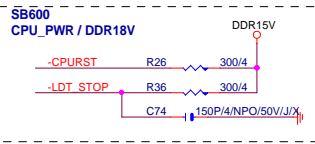




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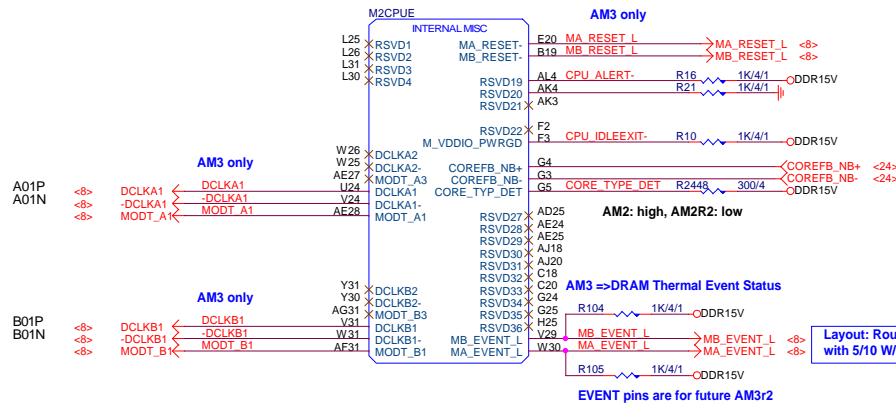
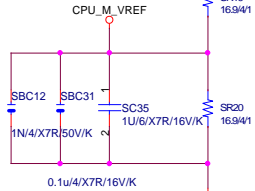
CPU DDRII MEMORY

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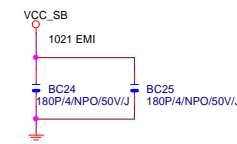
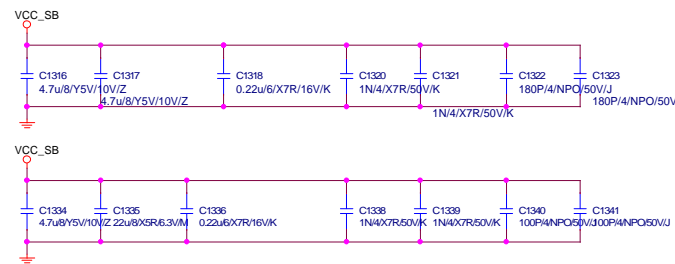
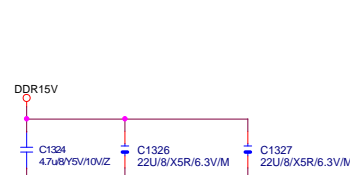
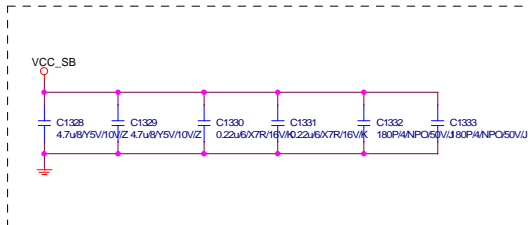
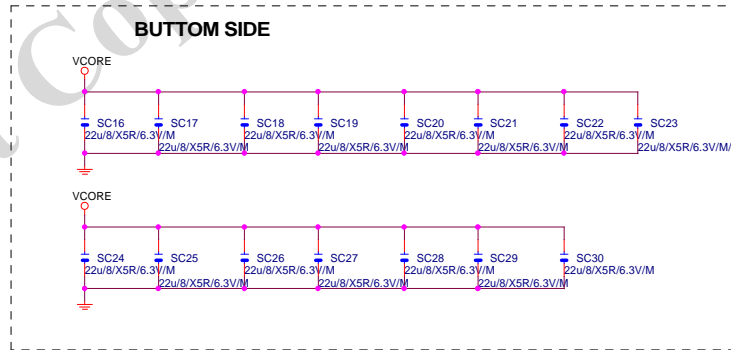
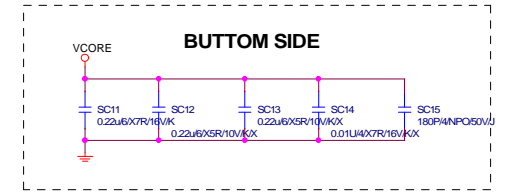
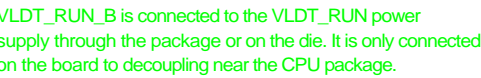
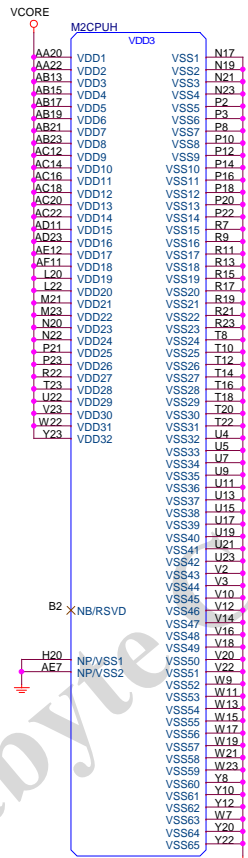
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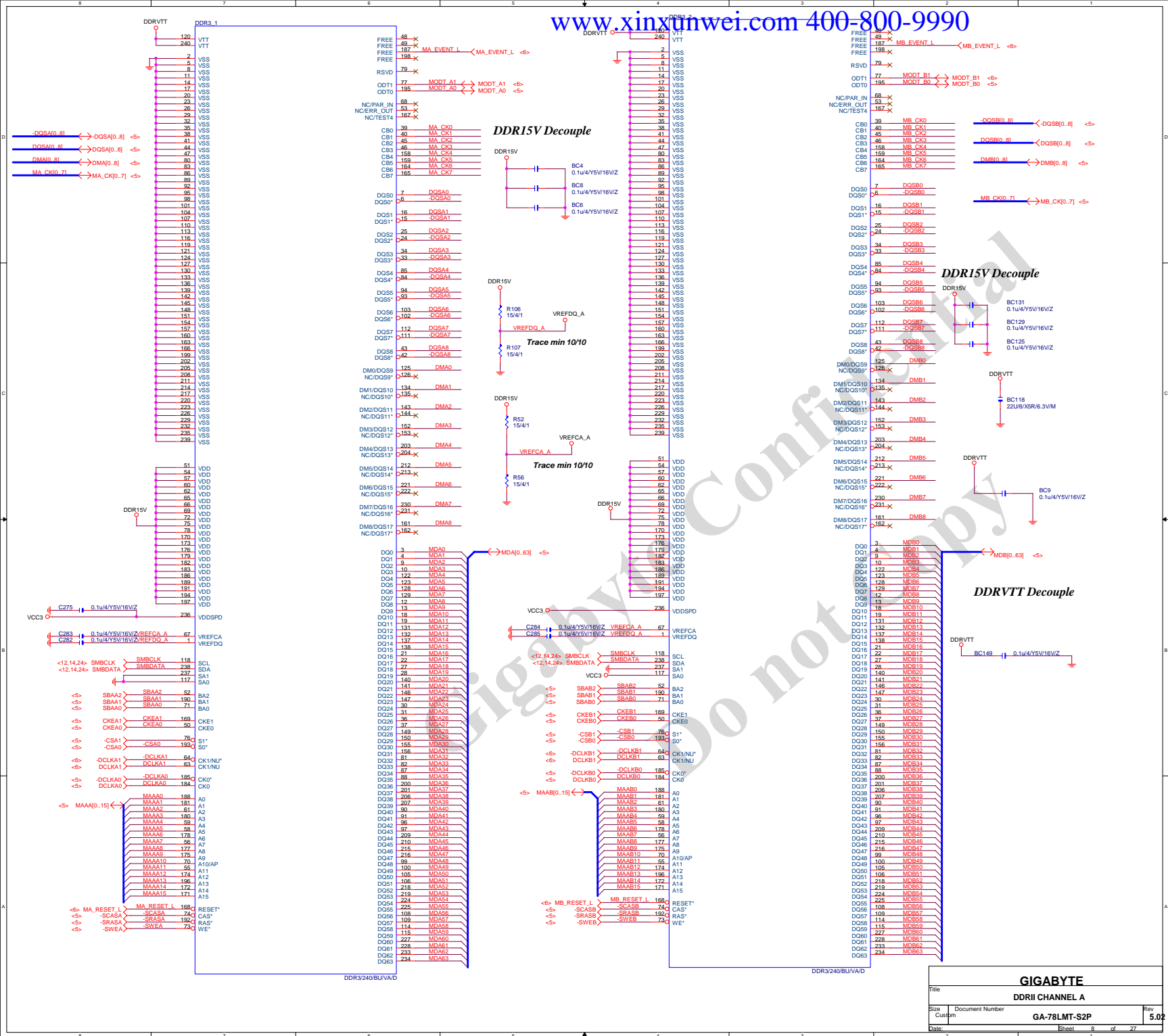
40 MILS WIDTH



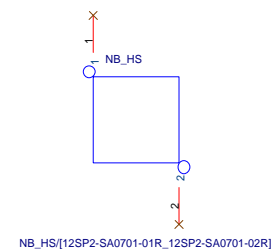
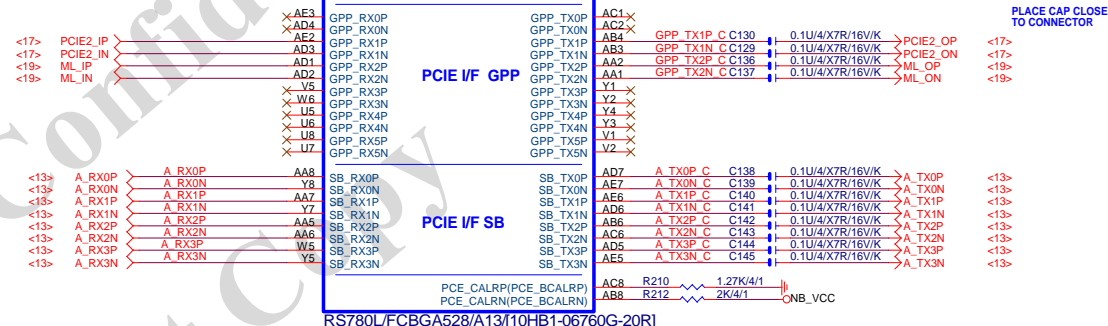
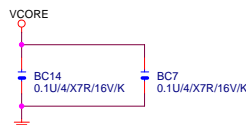
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PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP33	+3.3V	NC	NC

GROUND

RS780L/FCBGA528/A13[10HB1-06/60G-20R]

Please use 1mm pad size,  
place all ELT test pads  
on bottom side only

PART 5/6

POWER

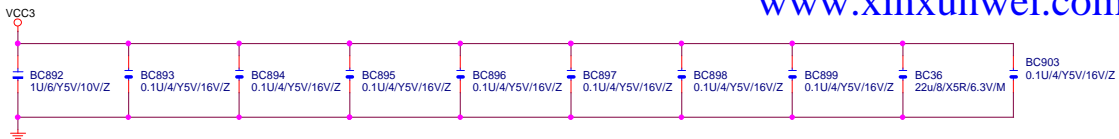
POWER

RS780L/FCBGA528/A13[10HB1-06/60G-20R]

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Title  
RS780 POWER & GNDSize  
Custom  
Document Number  
GA-78LMT-S2PRev  
5.02

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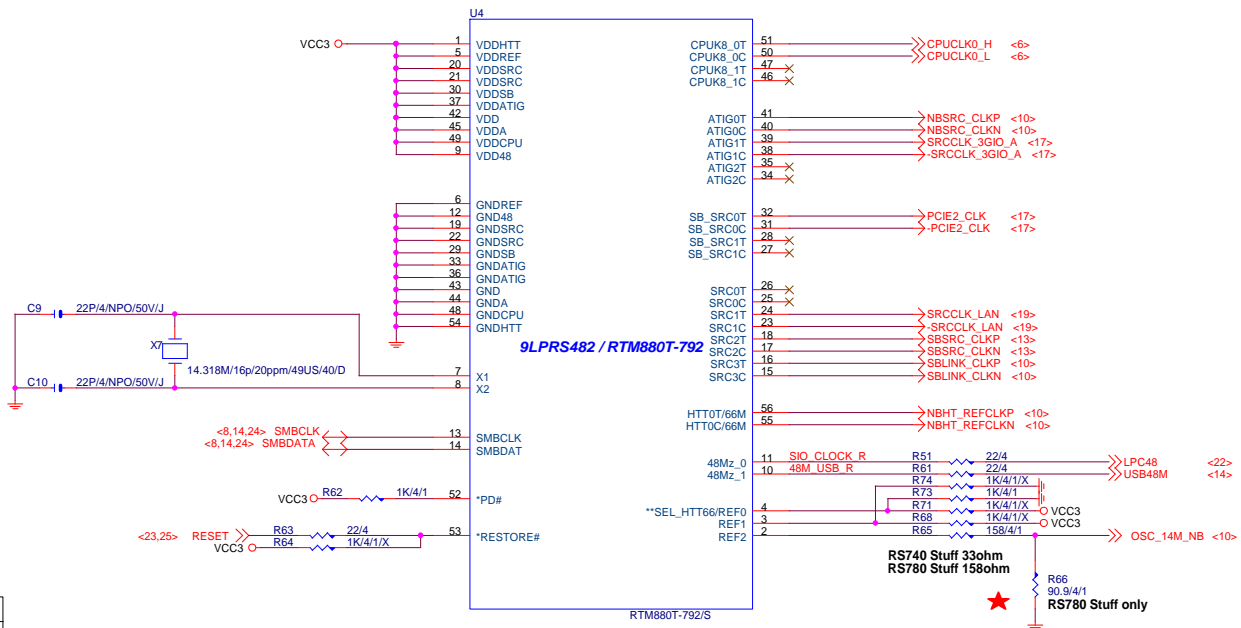


- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB\_C003 INPUT TABLE

NB_C003	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* the GFX\_REFCLK input is required for all cases



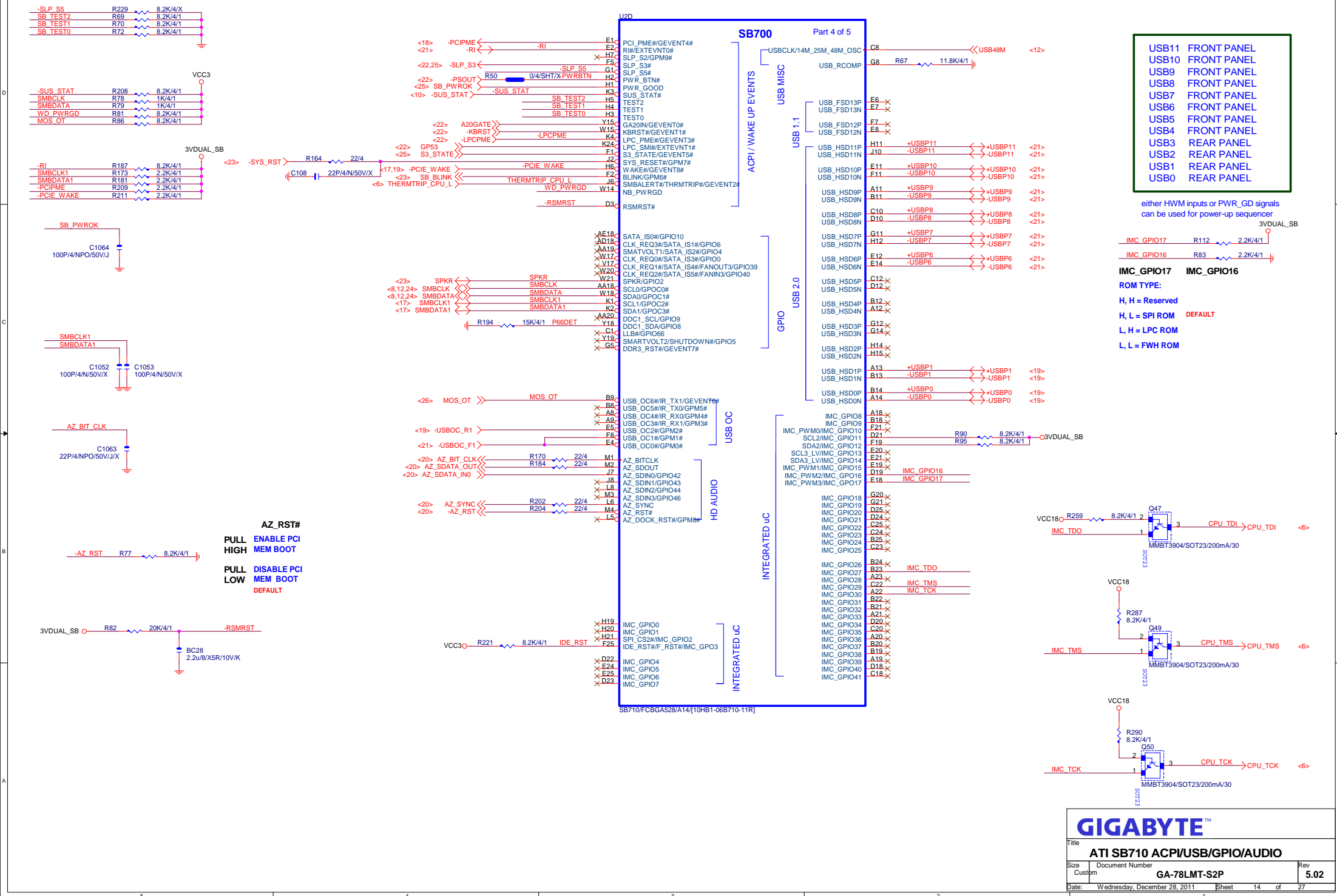
	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

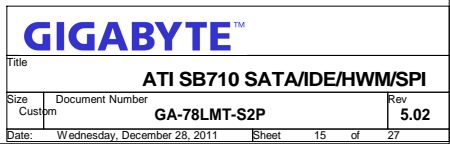
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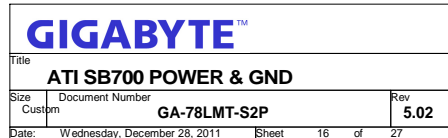
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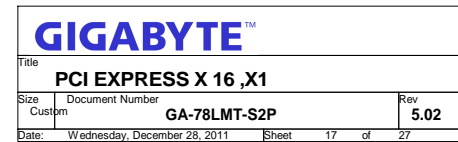
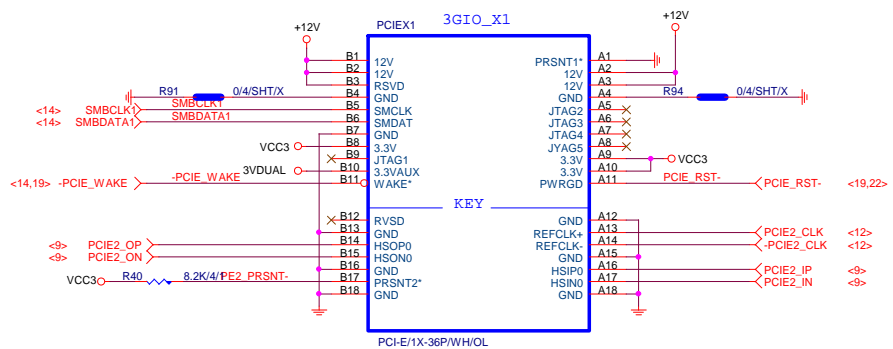






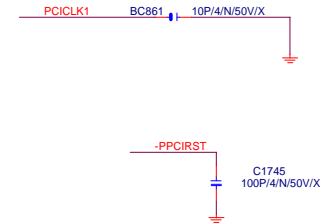
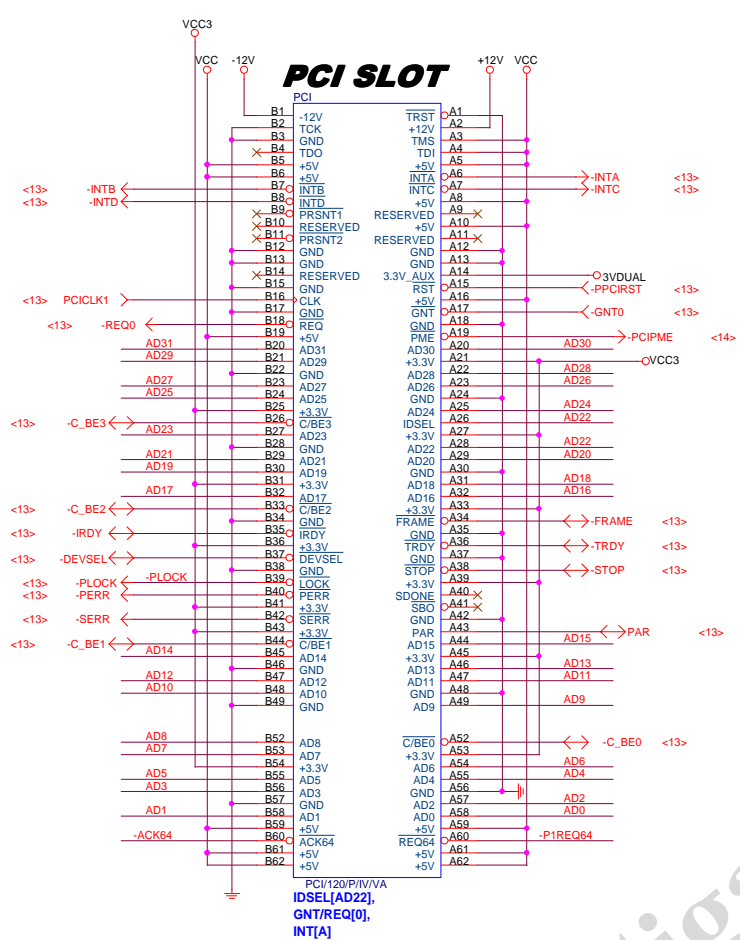




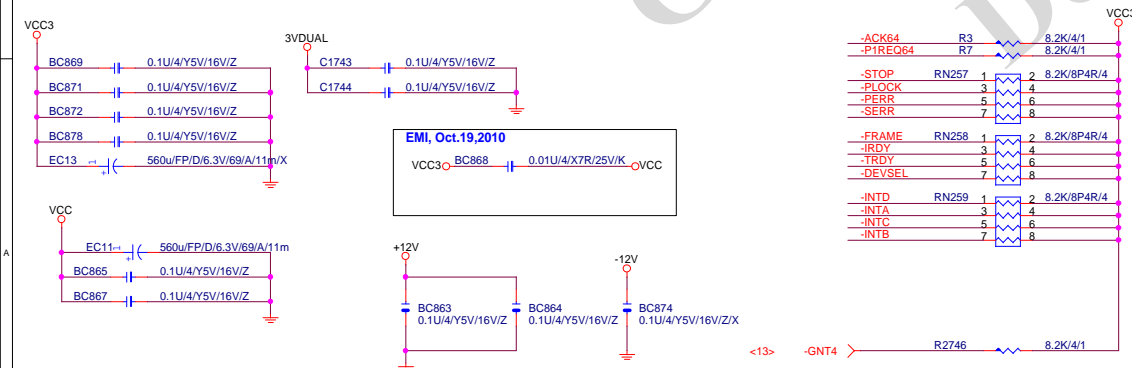


## PCI SLOT 1,2

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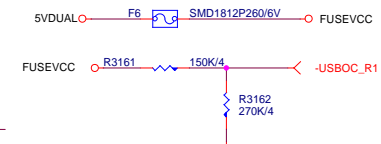
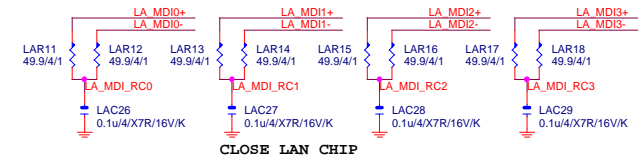
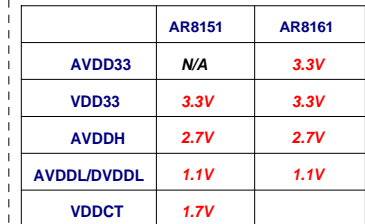


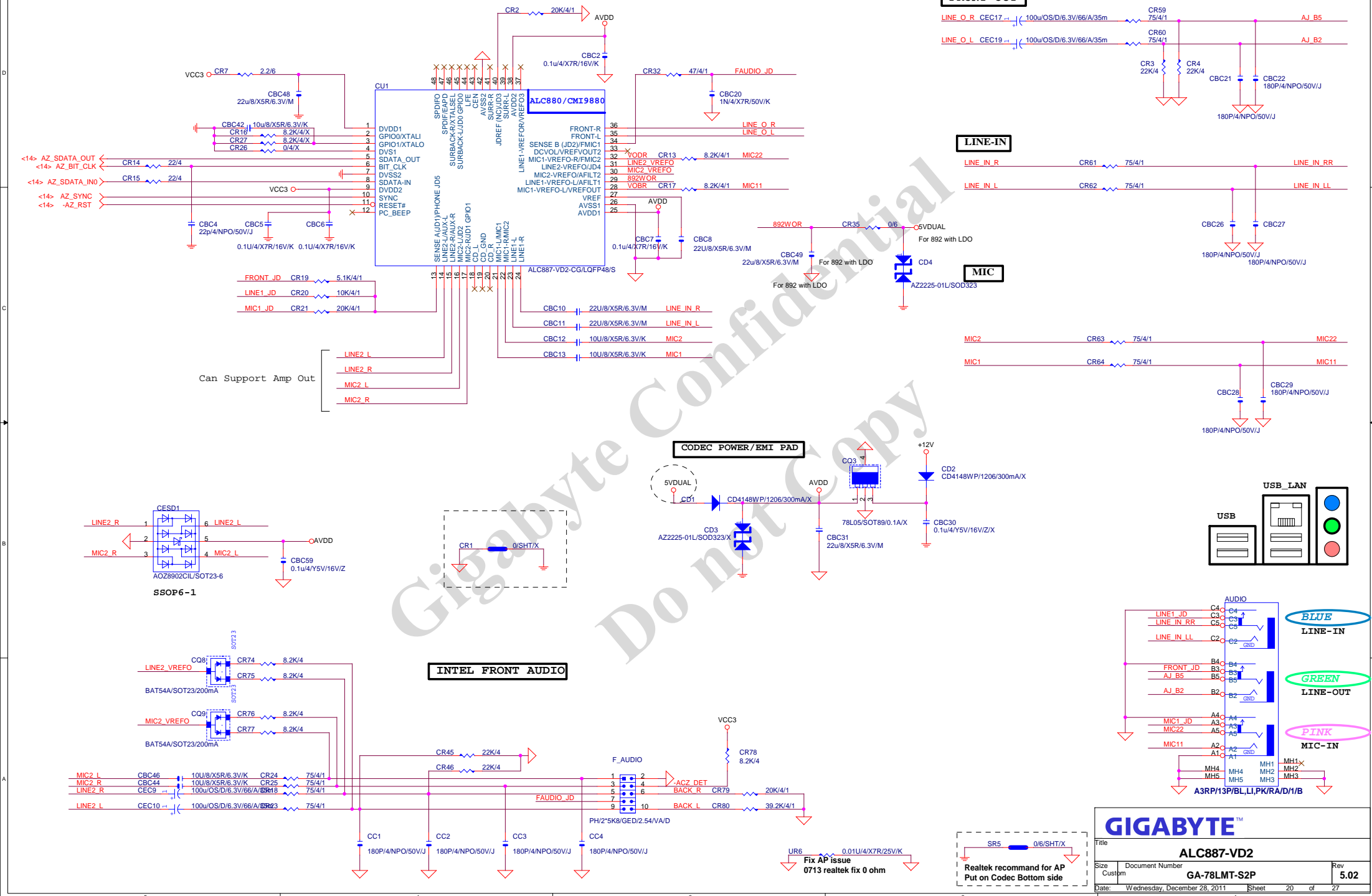
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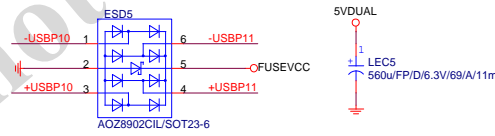
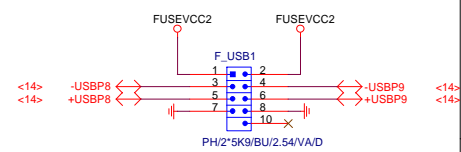
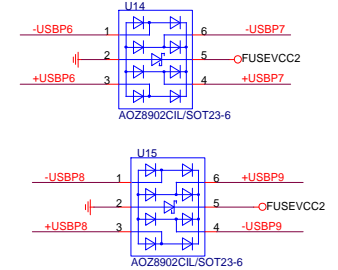
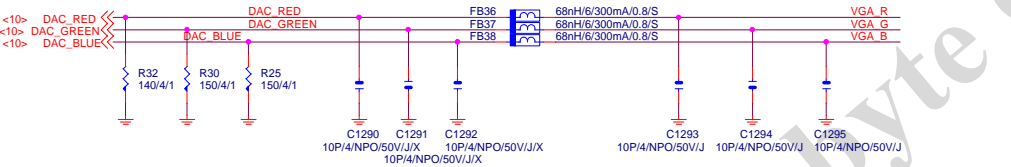
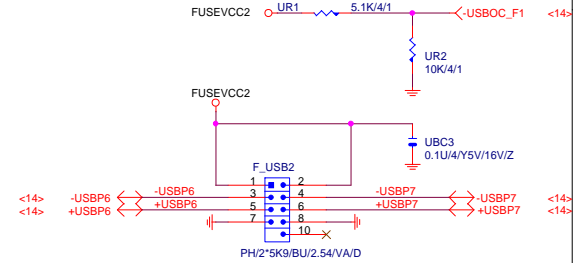
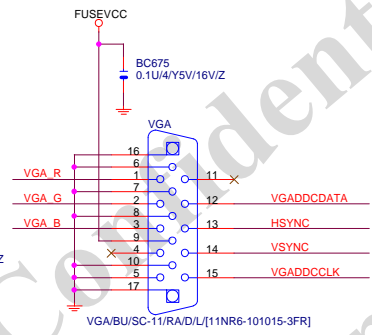
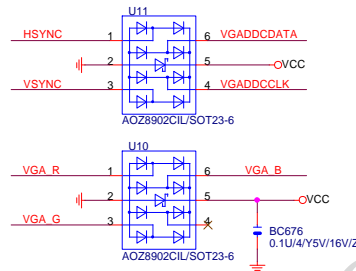
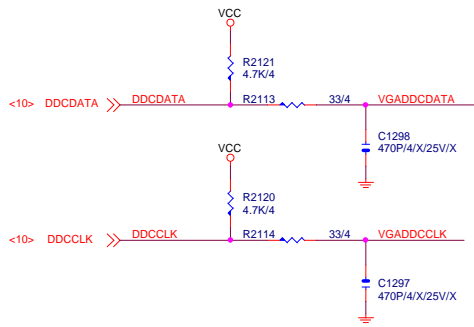
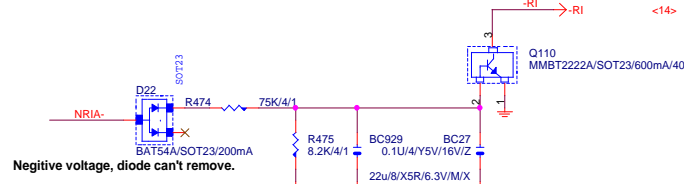


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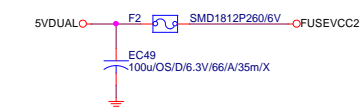
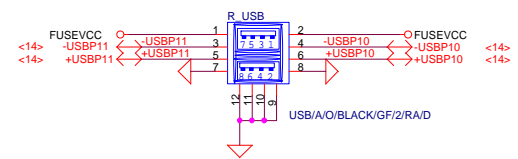
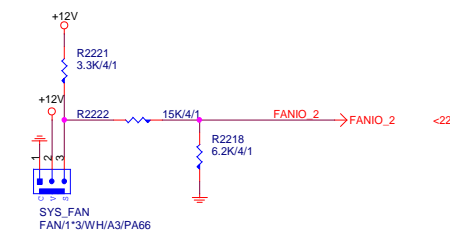
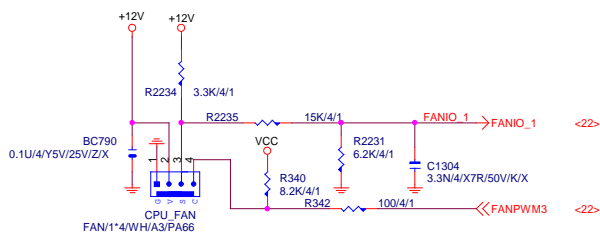
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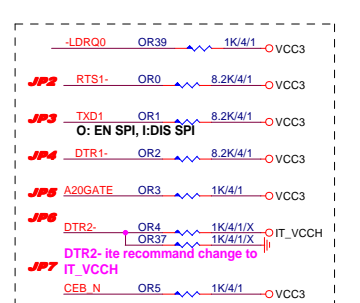
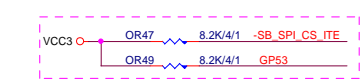
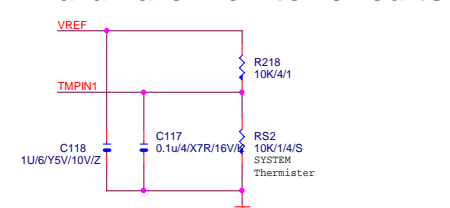
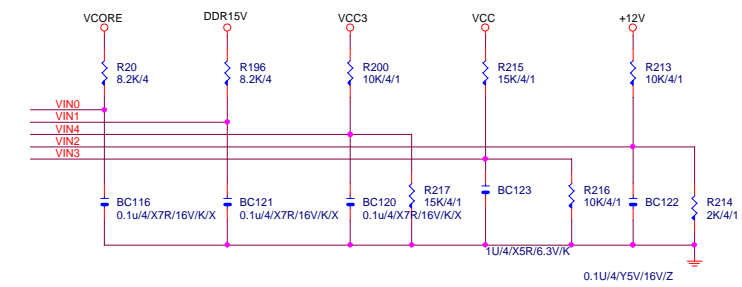
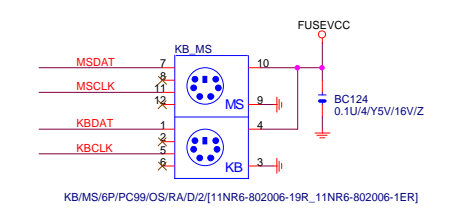
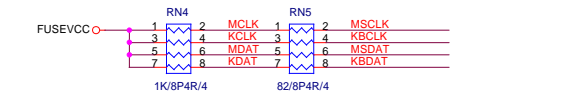
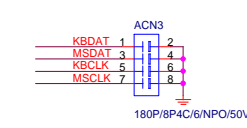
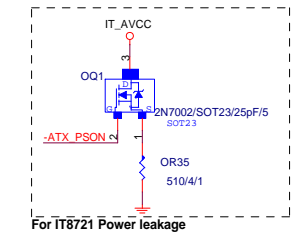


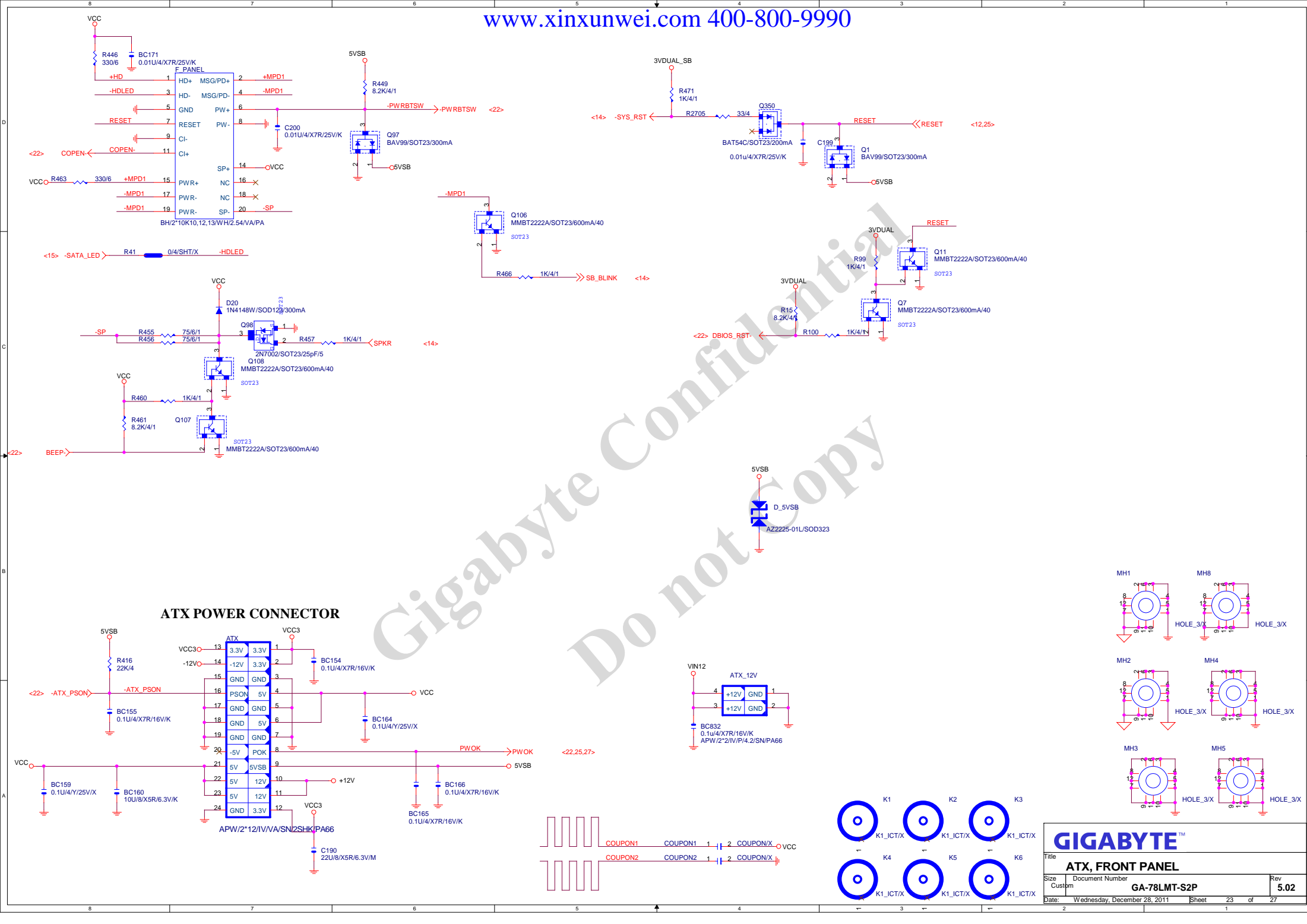




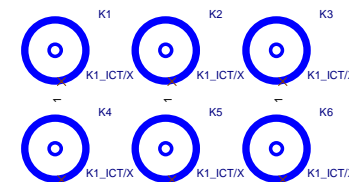
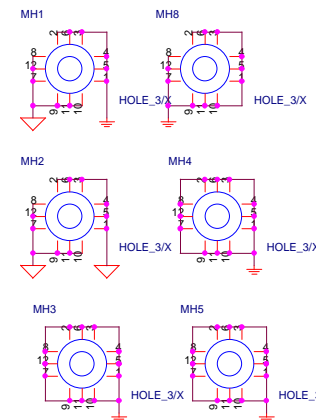
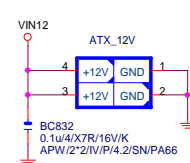
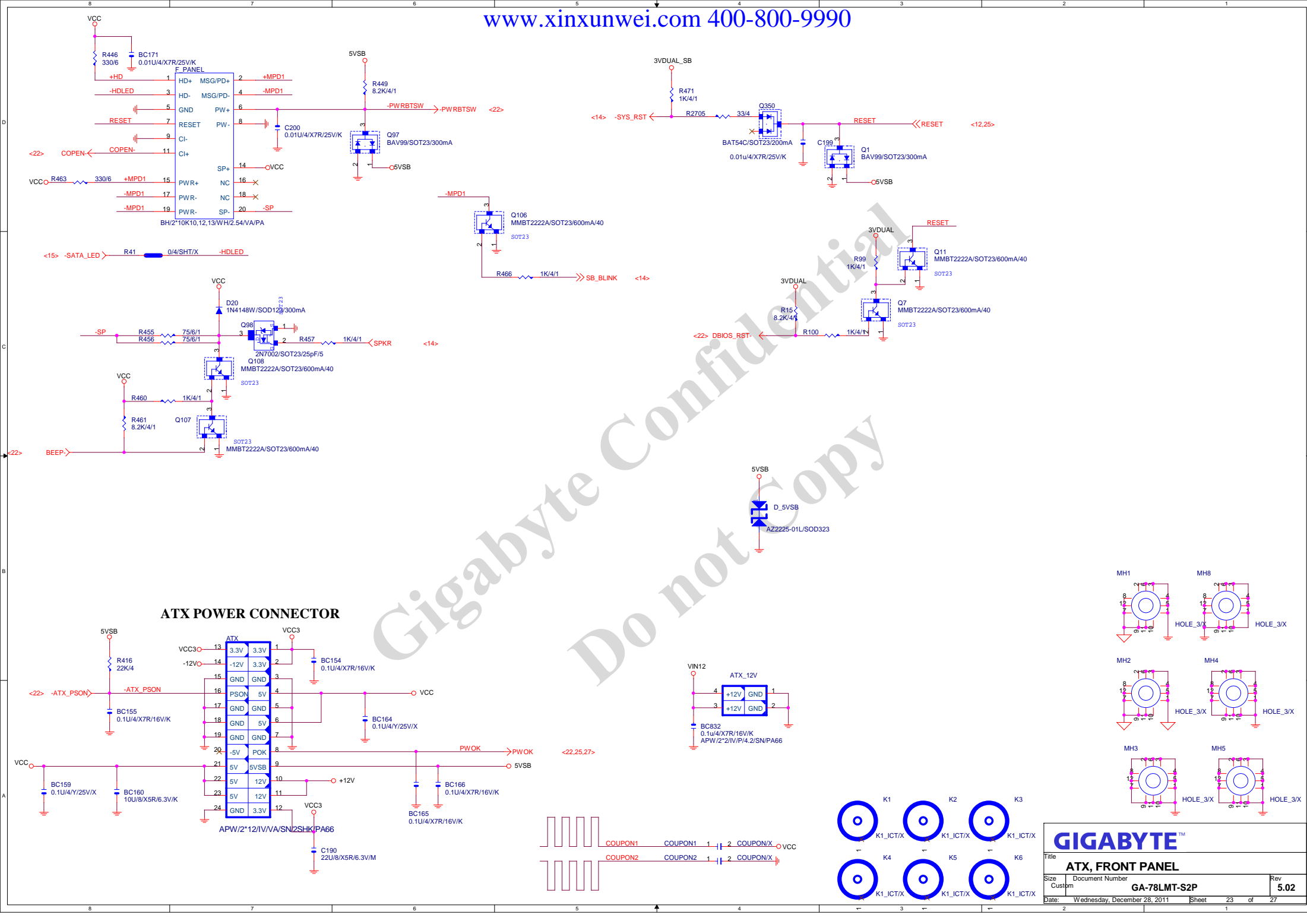
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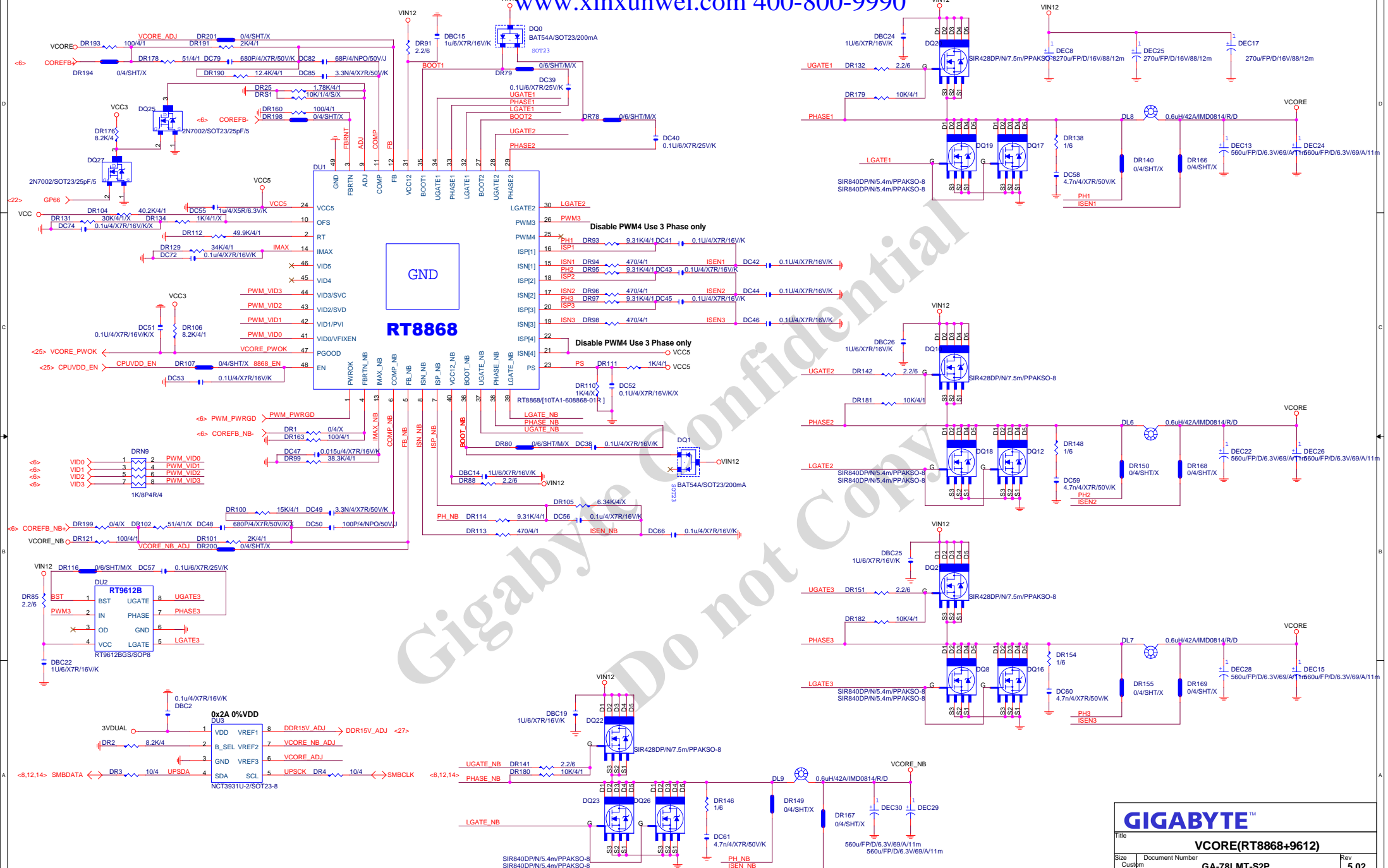


## ATX POWER CONNECTOR

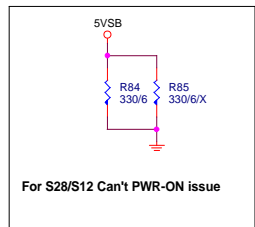
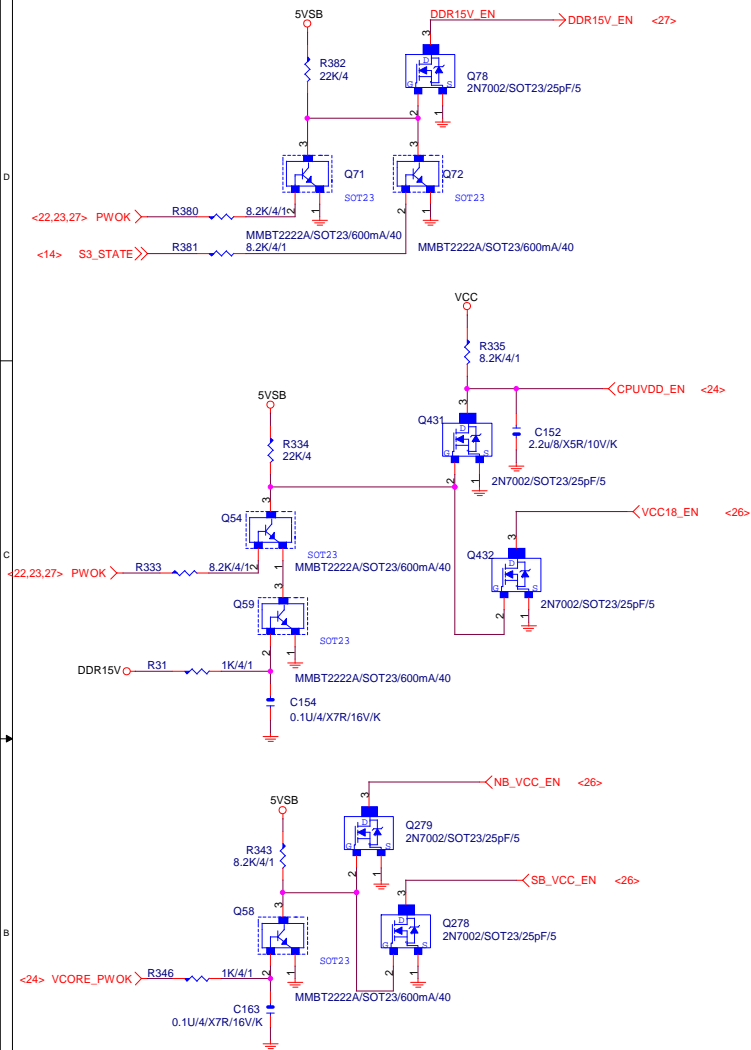


				
Title				
ATX, FRONT PANEL				
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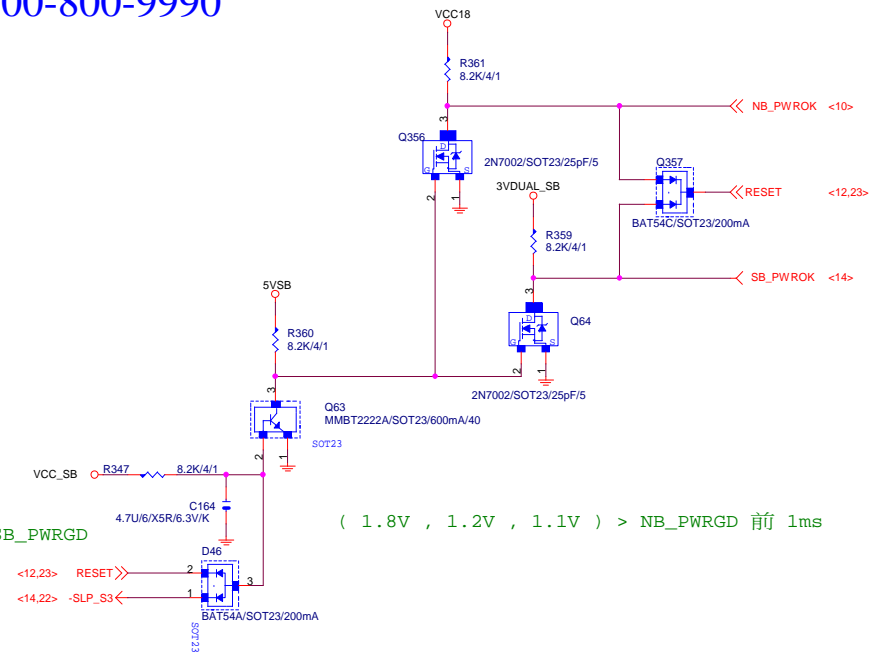








PWOK > NB\_PWRGD / SB\_PWRGD



( 1.8V , 1.2V , 1.1V ) > NB\_PWRGD 前 1ms

